nedeljainformatike v8.0

Jezici za opis hardvera

Luka Simić

Matematička gimnazija

15. 05. 2023.

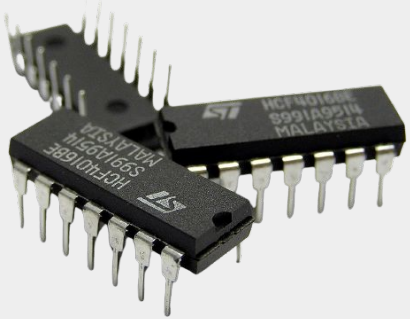
Agenda

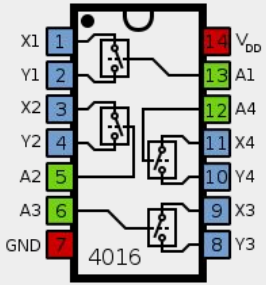
1. Motivacija
2. HDL jezici
3. Ostalo?

Motivacija – generalno

- Zašto uopšte pričati o ovome?

Integrisana kola

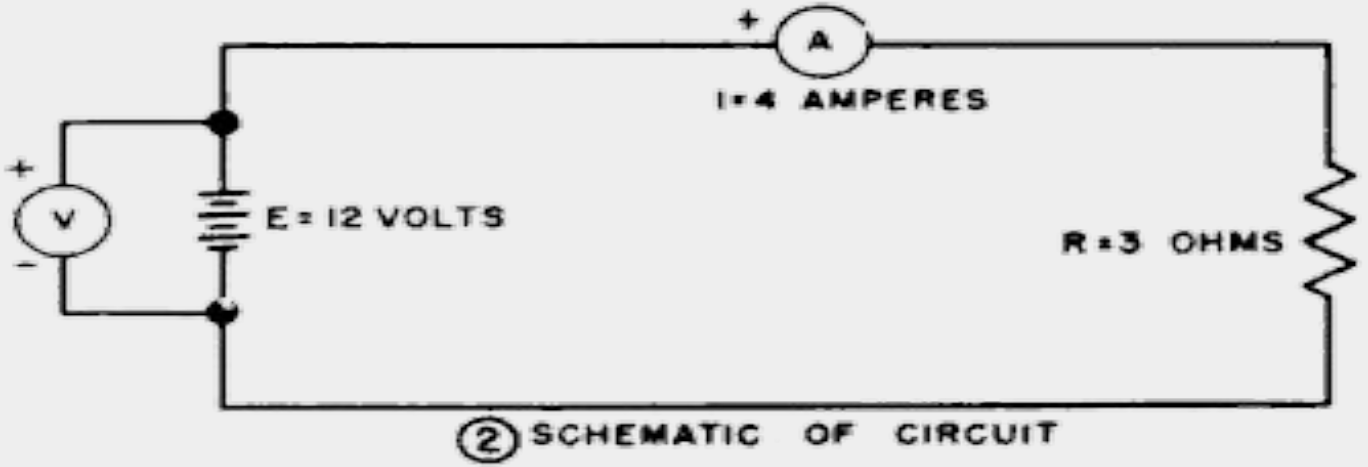




Ciklus razvoja

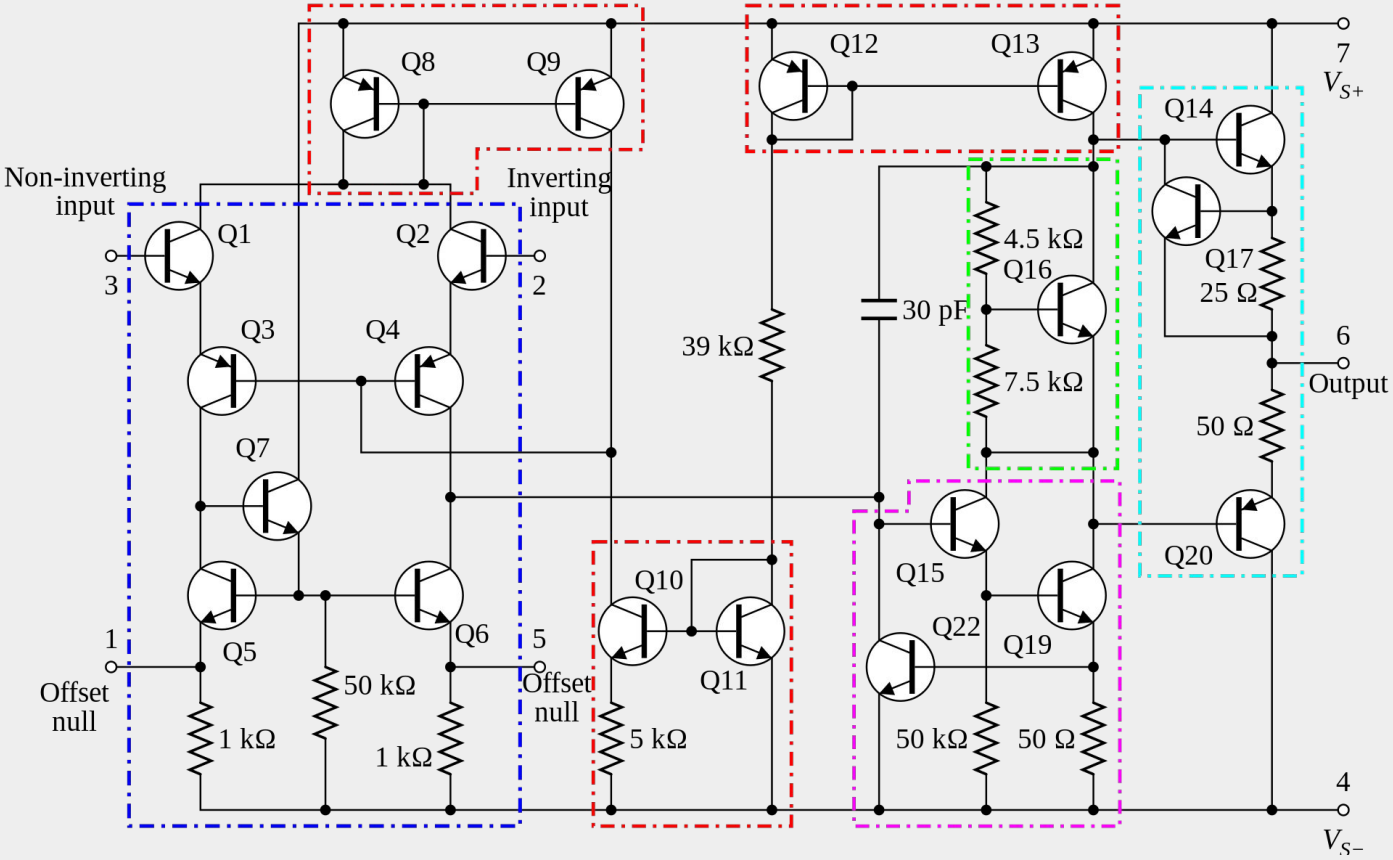
- **Softver:**
  - Planiranje
  - Analiza
  - Dizajn
  - Implementacija
  - Testiranje
  - Održavanje
  - ...
- **Hardver:**
  - Specifikacija
  - Arhitektura
  - Dizajn
  - Verifikacija
  - *Layout*
  - Fabrikacija
  - Validacija

Šta će nam?

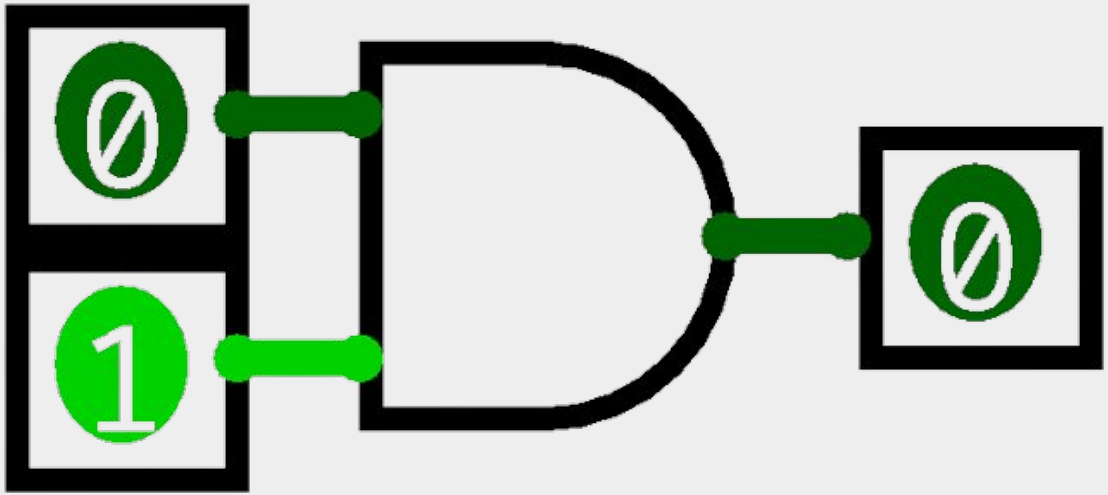


② SCHEMATIC OF CIRCUIT

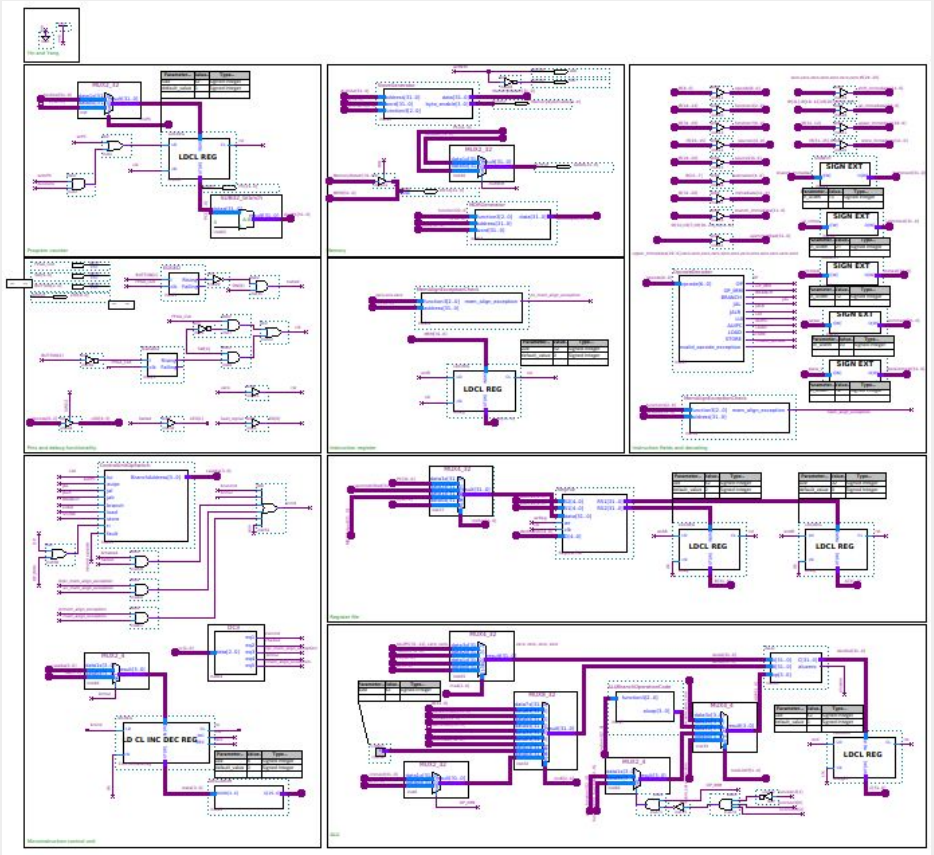
Šta će nam?


Non-inverting input
3
Inverting input
2
Offset null
1
Offset null
5
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q19
Q20
Q22
1 kΩ
50 kΩ
1 kΩ
5 kΩ
39 kΩ
30 pF
4.5 kΩ
7.5 kΩ
25 Ω
50 Ω
50 kΩ
50 Ω
7
V_{S+}
6
Output
4
V_{S-}

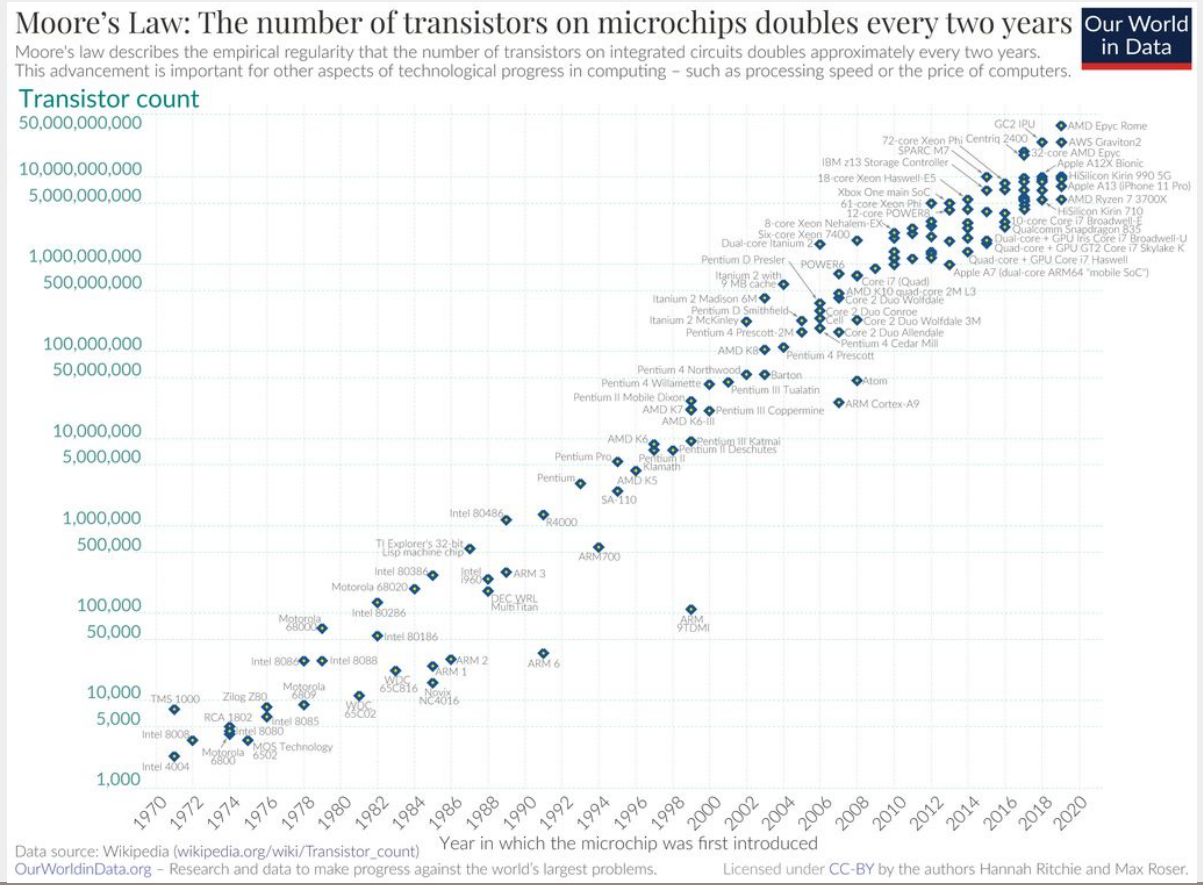
Šta će nam?



Šta će nam?



Murov zakon


Moore's Law: The number of transistors on microchips doubles every two years
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years.
This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.
Our World in Data
Transistor count
50,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
5,000
1,000
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
2018
2020
Year in which the microchip was first introduced
Intel 4004
Intel 8008
Intel 8080
Intel 8085
MOS Technology 6502
Motorola 6800
Motorola 6809
Zilog Z80
RCA 1802
TMS 1000
WDC 65C02
WDC 65C816
Intel 8086
Intel 8088
ARM 1
ARM 2
Intel 80186
Intel 80286
Motorola 68000
Motorola 68020
Intel 80386
Intel i960
ARM 3
TI Explorer's 32-bit Lisp machine chip
DEC WRL MultiTitan
ARM 6
ARM 9TDMI
Intel 80486
R4000
ARM700
Pentium
AMD K5
SA-110
Pentium Pro
Pentium II Klamath
AMD K6
Pentium II Deschutes
Pentium III Katmai
AMD K6-III
AMD K7
Pentium III Coppermine
Pentium 4 Willamette
Pentium 4 Northwood
Barton
Pentium III Tualatin
Pentium II Mobile Dixon
ARM Cortex-A9
Atom
AMD K8
Pentium 4 Prescott
Pentium 4 Cedar Mill
Itanium 2 McKinley
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Cell
Core 2 Duo Conroe
Core 2 Duo Wolfdale 3M
Itanium 2 Madison 6M
Pentium D Smithfield
Core 2 Duo Wolfdale
AMD K10 quad-core 2M L3
Itanium 2 with 9 MB cache
Core i7 (Quad)
Pentium D Presler
POWER6
Dual-core Itanium 2
Six-core Xeon 7400
8-core Xeon Nehalem-EX
12-core POWER8
Xbox One main SoC
61-core Xeon Phi
18-core Xeon Haswell-E5
i8M z13 Storage Controller
SPARC M7
72-core Xeon Phi
Centriq 2400
GC2 IPU
AMD Epyc Rome
AWS Graviton2
32-core AMD Epyc
Apple A12X Bionic
HiSilicon Kirin 990 5G
Apple A13 (iPhone 11 Pro)
AMD Ryzen 7 3700X
HiSilicon Kirin 710
10-core Core i7 Broadwell-E
Qualcomm Snapdragon 835
Dual-core + GPU Iris Core i7 Broadwell-U
Quad-core + GPU GT2 Core i7 Skylake K
Quad-core + GPU Core i7 Haswell
Apple A7 (dual-core ARM64 "mobile SoC")
Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldinData.org – Research and data to make progress against the world's largest problems.
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Agenda

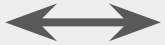
1. Motivacija
2. HDL jezici
3. Ostalo?

Razlike od programskih jezika

- Ne izvršavaju se na procesoru
- Moraju da se pretvore u hardver
- Nisu proceduralni

Primeri

```
module and_2 (
    input in1,
    input in2,
    output out
);
    assign out = in1 & in2;
endmodule
```



```
bool and_2 (
    bool in1,
    bool in2
) {
    return in1 && in2;
}
```

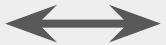
Primeri

```
module mux_2 (
    input [31:0] i0,
    input [31:0] i1,
    input control,
    output [31:0] out
);
    assign out = control ?
        i1 :
        i0;
endmodule
```

```
int mux_2 (
    int i0,
    int i1,
    bool control
) {
    return control ?
        i1 :
        i0;
}
```

Primeri

```
module mux_2 (
    input [31:0] i0,
    input [31:0] i1,
    input control,
    output reg [31:0] out
);
    always @(*) begin
        if (control == 1'b0)
            out = i0;
        else
            out = i1;
    end
endmodule
```



```
int mux_2 (
    int i0,
    int i1,
    bool control
) {
    int out;
    if (control == 0)
        out = i0;
    else
        out = i1;
    return out;
}
```

Primeri

```
module red (
    input clk,
    input in,
    output reg out
);
    reg prev;
    always @(posedge clk) begin
        prev <= in;
        out <= (in == 1'b1) && (prev == 1'b0);
    end
endmodule
```

Primeri

```
module red (
    input clk,
    input in,
    output reg out
);
    reg prev;
    always @(posedge clk) begin
        prev <= in;
        out <= (in == 1'b1) && (prev == 1'b0);
    end
endmodule
```

Primeri

```
module red (
    input clk,
    input in,
    output reg out
);
    reg prev;
    Reg i
    always @(posedge clk) begin
       For (i +)
    end
endmodule
```

Agenda

1. Motivacija
2. HDL jezici
3. Ostalo?

Hvala na pažnji!

Pitanja?